circuit, while the first $N^{++}$ layer **6** is connected to a lowest-potential terminal of the semiconductor integrated circuit.

**[0046]** In the electrostatic discharge (ESD) protection device thus constituted, the field oxide film **8** is formed so as to overlap with the region of the high-density N-type sink layer **3** by at least a certain area. In other words, the high-density N-type sink layer **3** is formed in such a manner that extends from the second $N^{++}$ layer **7** through the region below the field oxide film **8**.

**[0047]** A more detailed aspect is given below. A thickness of the N-type epitaxial layer **2** is approximately 4.2 μm. The high-density N-type sink layer **3** is formed from the surface of the N-type epitaxial layer **2** up until a position in a depth of approximately 3.5 μm, and a peak density thereof is approximately $3\times10^{17}/cm^3$. A depth of the $P^-$ layer **4** is approximately 2.0 μm from the surface of the N-type epitaxial layer **2**, and a peak density thereof is approximately $6\times10^{16}/cm^3$. A depth of the $P^+$ layer **5** is approximately 0.5 μm, and a peak density thereof is approximately $2.0\times10^{17}/cm^3$. A depth of the first $N^{++}$ layer **6** is approximately 0.2 μm, and a peak density thereof is approximately $2.5\times10^{20}/cm^3$. A depth of the second $N^{++}$ layer **7** is approximately 0.2 μm, and a peak density thereof is approximately $2.5\times10^{20}/cm^3$. A region width X where the high-density N-type sink layer **3** and the field oxide film **8** overlap with each other (extended dimension of the high-density N-type sink layer **3** expanding from a border between the second $N^{++}$ layer **7** and the field oxide film **8** up until below the field oxide film **8**) is 10-40 μm.

**[0048]** An operation of the transistor having the foregoing structure is described below. First, when a surge is applied to the collector, breakdown is caused between the $P^-$ layer **4** and the high-density N-type sink layer **3** in the case where a withstand voltage determined by the separation between them exceeds the predetermined value. Based on a breakdown current thereby generated, the operation of the NPN transistor constituting the electrostatic discharge protection device according to the present preferred embodiment is started, and the current flows from the collector to the emitter. At the time, the current flow by the transistor operation passes from the second $N^{++}$ layer **7** through the region of the high-density N-type sink layer **3** below the field oxide film **8**, and further flows to the emitter via the route of N-type epitaxial layer **2**→$P^-$ layer **4**→$P^+$ layer **5**→first $N^{++}$ layer **6**.

**[0049]** Here, a built-in resistor having a sufficiently large value is formed in the high-density N-type sink layer **3** through making the region width X larger, which generates voltage drop. Therefore, the retained voltage Vh is made to be a higher voltage in comparison to the case where the high-density N-type sink layer **3** is not provided below the field oxide film **8**.

**[0050]** In order to confirm the effect of the present invention based on the recognition that the retained voltage Vh is improved as the region width X is increased, the region width X was changed under a state where the separation between the high-density N-type sink layer **3** and the $P^-$ layer **4** shown in FIG. **1** was maintained at a certain level, and the change of the retained voltage Vh was simulated based on an actual measurement. The measurement and the simulation were implemented by means of the TLP (Transmission Line Pulse). The result is shown in FIG. **2**. FIG. **2** shows the snap-back characteristic in the different region widths X, based on an assumption that the horizontal axis denotes the collector voltage and the vertical axis denotes the collector current.

**[0051]** As shown in FIG. **2**, when the region width X is 0 μm, the retained voltage Vh is reduced to at most 40 V. On the contrary, when the region width X is at least 10 μm, the retained voltage Vh holds at least 40 V because the built-in resistor formed in accordance with the region width X is serially connected to the collector of the NPN transistor. Focusing on the transistor operation region (0.5 A-3.5 A) after the retained voltage Vh shown in FIG. **2**, the tilt of the snap-back characteristic is increased as the region width X is increased.

**[0052]** As described above, a higher voltage of the retained voltage Vh is achieved according to the present invention, and the ESD protection device of the NPN transistor free of any restriction from a voltage range can be provided in the integrated circuit having the high voltage resistance.

Second Preferred Embodiment 2

**[0053]** In the preferred embodiment 1, improvement of the retained voltage Vh is tried by expanding the region width X of the high-density N-type sink layer **3** below the field oxide film **8**. However, it is necessary to set the region width X to at least 10 μm in order to be secured of the retain voltage Vh of at least 40 V as shown in FIG. **2**.

**[0054]** In the case where use of the ESD protection device is desired in the range of higher voltages, it is necessary to further broaden the region width X. When use of the ESD protection device is tried in the region of the power-supply voltage of 50V, for example, it is necessary for the region width X to be at least 50 μm, which means that the cell area of the ESD protection device is increased to at least 50 μm in the horizontal direction. Therefore, the area of the ESD protection device occupied in the entire area of the chip is increased, and the chip size may be unfavorably increased in the constitution according to the preferred embodiment 1.

**[0055]** A structure according to a preferred embodiment 2 of the present invention, that can dispel such anxiety, is described referring to FIG. **3**. This is the structure for making the resistance formed in the high-density N-type sink layer **3** below the field oxide film **8** to be much higher value. A P-type layer **9** is formed on the surface in at least a partial region of the high-density N-type sink layer **3** below the field oxide film. The P-type layer **9** constitutes a fifth diffusion layer of the first conductivity type. As shown in FIG. **3**, it is preferable that the P-type **9** is arranged in the high-density N-type sink layer **3** below the field oxide film **8**. By doing this, a punch-through is formed with the P-type layer **9** and the $P^-$ layer **4**, and the voltage resistance between the collector and base can be prevented from decreasing.

**[0056]** According to the foregoing constitution, a pinch resistor is formed in the region of the high-density N-type sink layer **3** below the P-type layer **9**. The pinch resistor is serially connected to the collector of the transistor, and the retained voltage Vh is thereby further increased. As a result, the enlargement of the region of the high-density N-type sink layer **3** can be reduced to a minimum level, and the cell area can be thereby prevented from increasing.

**[0057]** In the preferred embodiments, the polarities (conductivity types) of the diffusion layers may be reversed. Further, the two diffusion layers, which are the $P^-$ layer **4** and the $P^+$ layer **5**, constitute the base, however, the effect of